PCB DESIGN GUIDELINES

Guidelines for the design and layout of high-speed digital logic PCBs.

- Give a lot of consideration to component placement and orientation.
- Avoid overlapping clock harmonics. Make a harmonic table for each clock.
- Clock signal loop area must be kept as small as possible. Get paranoid about clocks!
- Use multilayer boards with power & ground planes whenever possible.
- All high frequency signal traces must be on layers adjacent to a plane.
- Keep signal layers as close to the adjacent plane layer as possible (< 10 mils).
- Above 25 MHz PCB's should have two (or more) ground planes.
- When power & ground planes are on adjacent layers, the power plane should be recessed from the edge of the ground plane by a distance equal to 20 times the spacing between the planes.
- Bury clock signals between power & ground planes whenever possible.
- Avoid slots in the ground plane. Also applies to the power plane.
- If a segmented power plane is necessary, signal traces must not be routed over the slots.
- Filter (series terminate) the output of clock drivers to slow down their rise/fall times and to reduce ringing (typically 33 to 70 ohms).
- Place the clocks & high-speed circuitry as far away from the I/O area as possible.
- Use a minimum of two **equal value** decoupling capacitors on DIP packages, four on square packages. On high frequency/high power/noisy IC's many more capacitors may be necessary.
- Consider using embedded capacitance PCB structures for decoupling on h-f boards (>50 MHz)
- Use impedance-controlled PCB layout techniques (with proper terminations) where necessary
- On impedance-controlled PCBs, do not transition the signal from one layer to another unless both layers are referenced to the same plane.
- On non impedance-controlled PCBs, when a clock transitions from one layer to another & the layers are referenced to different planes add a transfer via or capacitor between the planes.
- All traces whose length (in inches) is equal to or greater than the signal rise/fall time (in nanoseconds) must have provision for a series-terminating resistor (typically 33 ohms).
- Simulate all nets whose length (in inches) is equal to or greater than the signal rise/fall time (in ns)
- Connect logic ground to the chassis (with a very low Z connection) in the I/O area. **This is crucial!**
- Provide for an additional ground to chassis connection at the clock/oscillator location.
- Additional ground to chassis connections may also be required.
- Daughter boards (with h-f, noisy devices and/or external cables) must be properly grounded to the motherboard and/or chassis (do not rely on the ground pins in the connector to provide this ground).
- Provide C-M filters on all I/O lines. Group all I/O lines together in a designated I/O area of the PCB.
- Shunt capacitors used in I/O filters must have a very low impedance connection to chassis.
- Use a power entry filter on the dc power line (both C-M & D-M)
- Most products in plastic enclosures need to be provided with an additional metal reference plane.
- Consider the use of board level component shields where applicable.
- Ground all heat sinks.

Note: Clock means any h-f periodic signal (e.g., CLK, RAS, CAS, ALE, etc.)

