PCB Design Conference - East
Keynote Address

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EMC ASPECTS OF FUTURE HIGH SPEED DIGITAL DESIGNS

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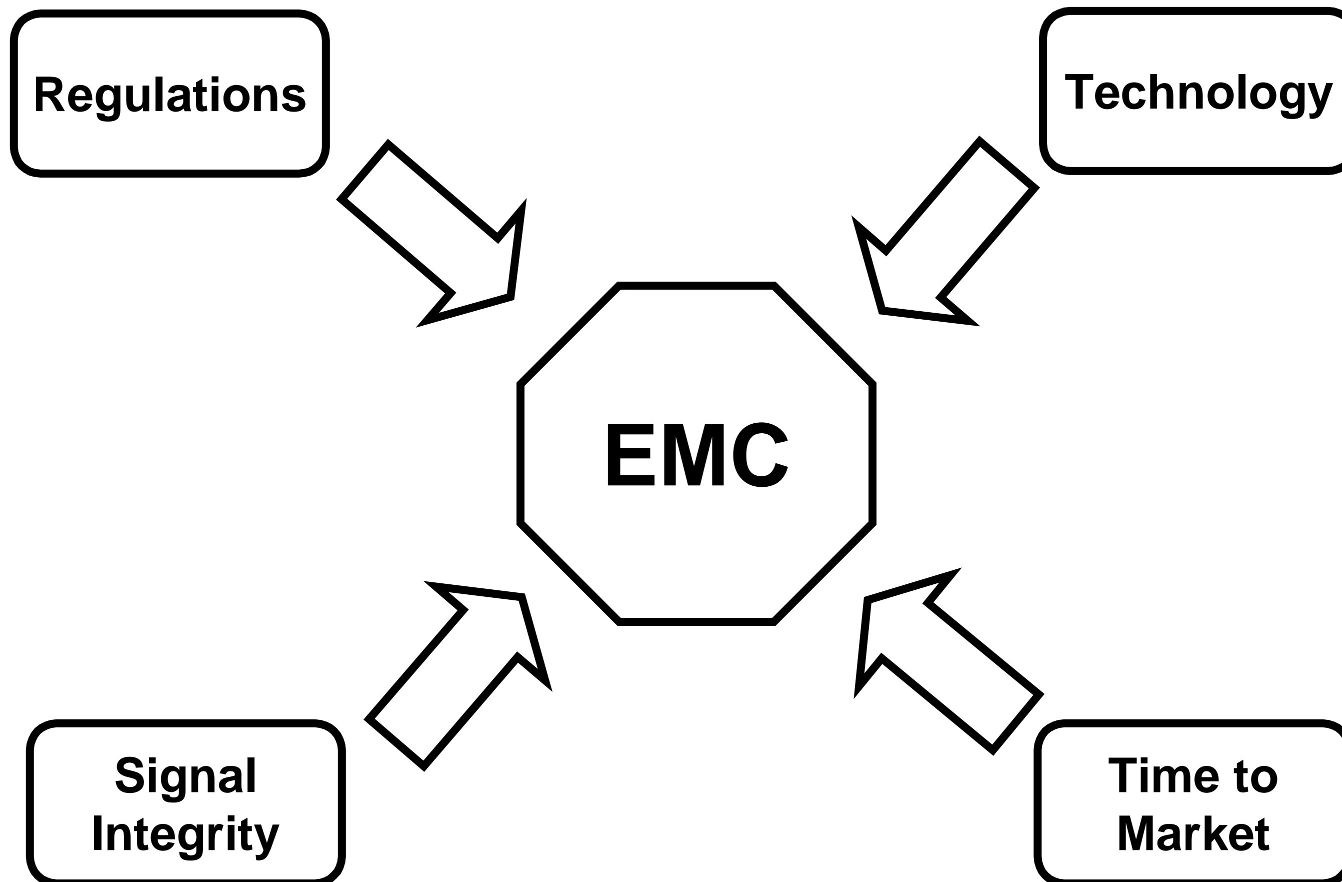
ELECTROMAGNETIC COMPATABILITY DRIVING FORCES



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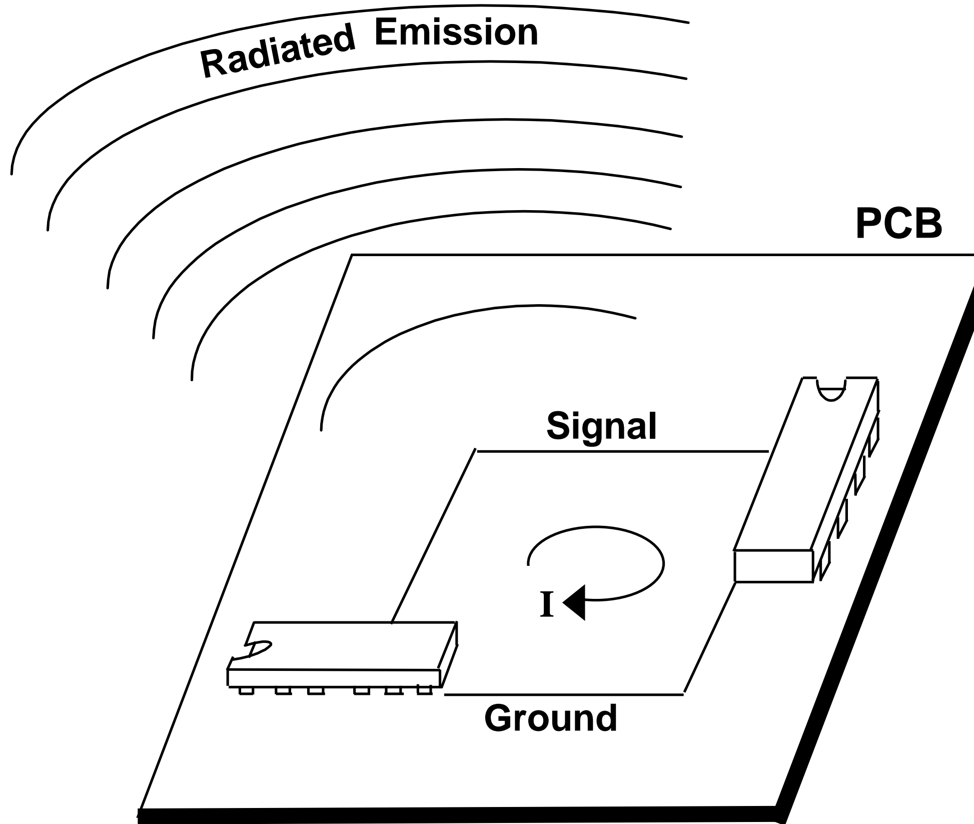
DIFFERENTIAL - MODE RADIATION



$$E = K_1 f^2 A I_0$$

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CONTROLLING DIFFERENTIAL-MODE EMISSIONS

- Reduce Loop Area
  - PCB Technology Has Not Keep Up With the Increase in Frequency Squared
- Cancellation Techniques
  - Canceling Clock Loops
  - Multiple Decoupling Capacitors
- Spread Spectrum Techniques
  - Clock Dithering

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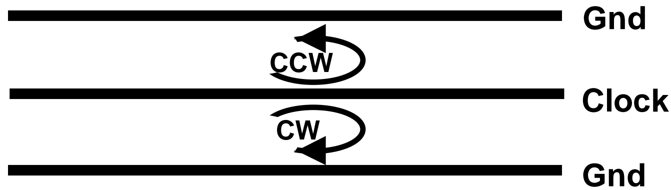
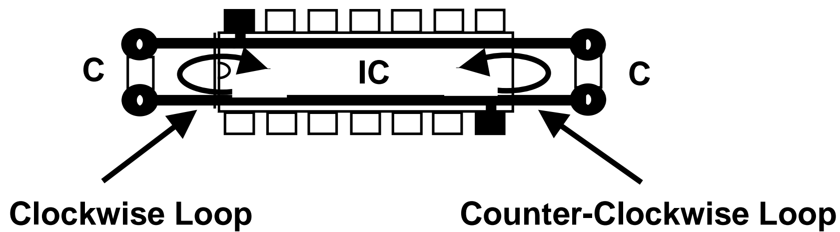
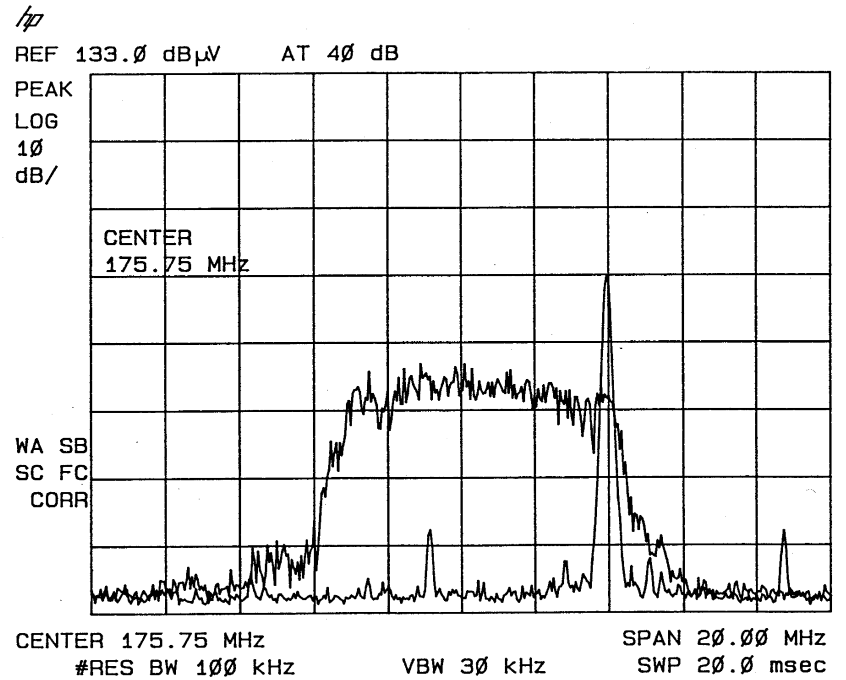
CANCELLATION TECHNIQUES





SPECTRUM OF A DITHERED CLOCK

(THIRD HARMONIC OF 60 MHz CLOCK)



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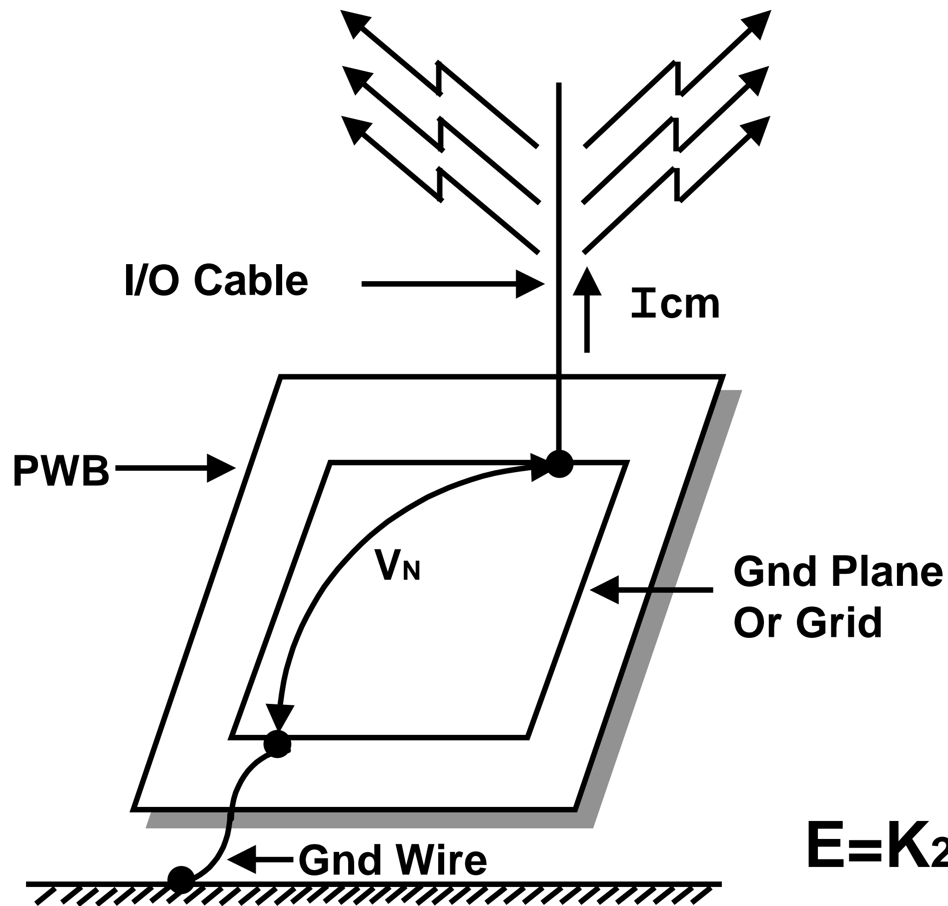
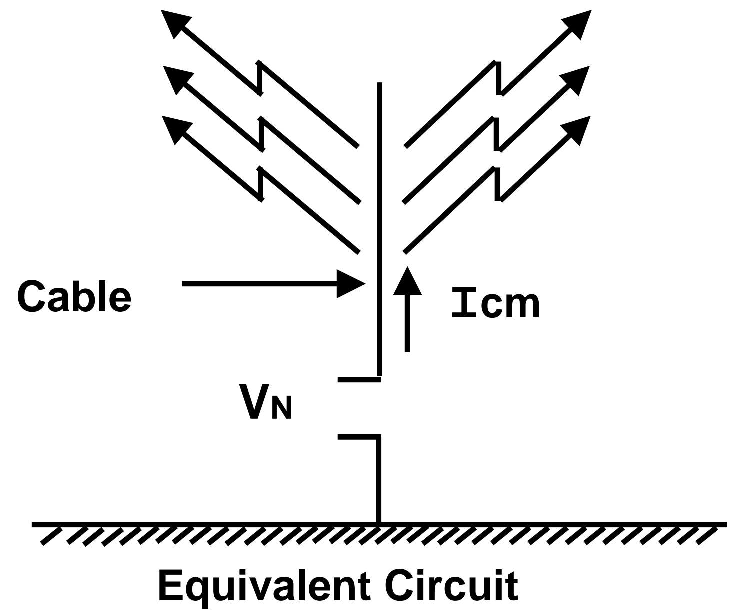
COMMON-MODE RADIATION



$$E = K_2 f L I_{cm}$$



Equivalent Circuit

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SKIN EFFECT

- Due to the Skin Effect, High Frequency Currents Can Only Penetrate a Metal a Very Small Distance
- Therefore, at High Frequencies all Currents are on the Surface of Conductors, and Cannot Penetrate them.

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GROUND RETURN CURRENTS

- Return Currents Will Always Flow on the Nearest Plane
- The Top and Bottom Surfaces of a Plane Act as Separate Conductors
- If The Top and Bottom Surfaces of a Plane Are Used for the Return Current,
  - How Does the Return Current Get From the Top to the Bottom of the Plane?
- If a Mixture of Power and Ground Planes are Used for the Return Current,
  - How Does the Return Current Get From One Plane to the Other?

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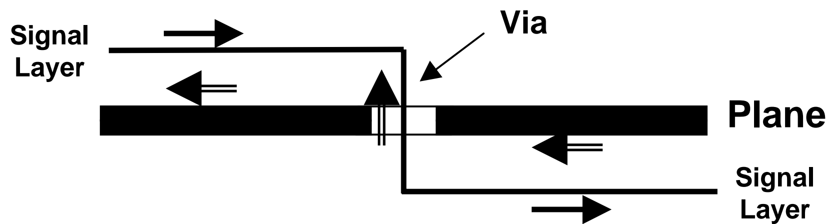
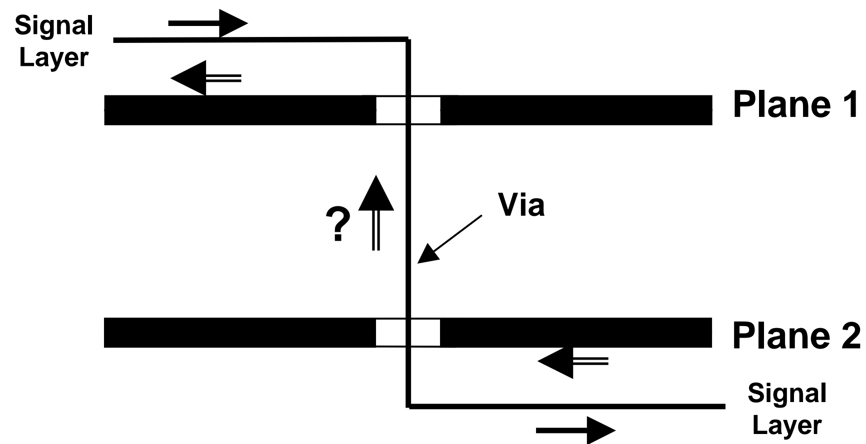
GROUND CURRENT FLOW



Signal Traces Adjacent to the Same Plane

OK



Signal Traces Adjacent to Different Planes

A Problem Unless We Do Something

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HIGH SPEED CLOCK ROUTING GUIDELINES
(in order of preference)

- Route Clock on One Layer Adjacent to a Plane
- Route Clock on Two Layers, Adjacent to the Same Plane
- Route Clock on Two Layers, Adjacent to Two Planes of the Same Type (i.e., Ground *or* Power) and Connect Planes Together With a Via Wherever there is a Signal Via
- Route Clock on Two Layers, Adjacent to Two Different Types of Planes (i.e., Ground *and* Power) and Connect Planes Together With a Decoupling Capacitor Wherever There is a Signal Via

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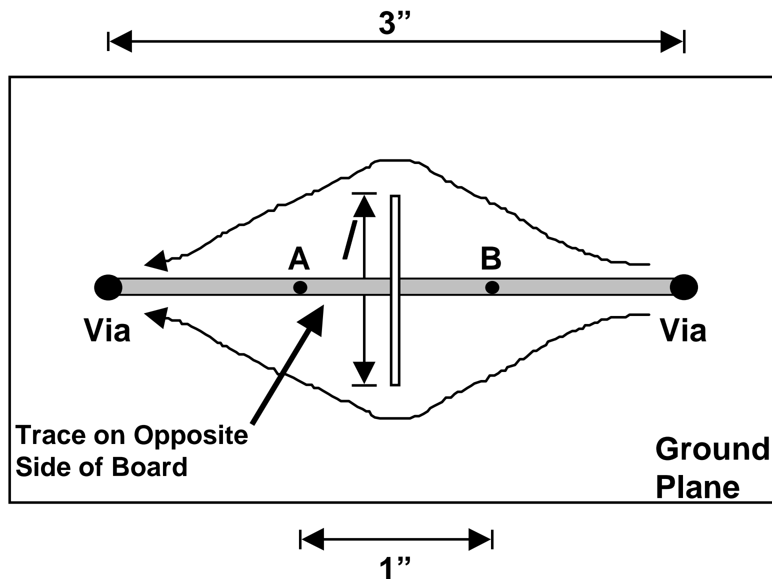
SLOT INDUCED GROUND PLANE VOLTAGE DROP
(3 nS RISE-TIME SQUARE WAVE)



l	V_{AB}	dB
0 in	15 mV	—
¼ in	20 mV	2.5
½ in	26 mV	4.8
1 in	49 mV	10.3
1½ in	75 mV	14.0
Holes	15+ mV	—

Notes:
- Slot is 0.025” Wide.
- Signal Trace Width is 0.050”.
- Holes = A Pattern of Fifteen 0.052” Diam. Holes Along a 1” Line

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We Must Learn To Ask The Question,

Where Does The Return Current Flow?

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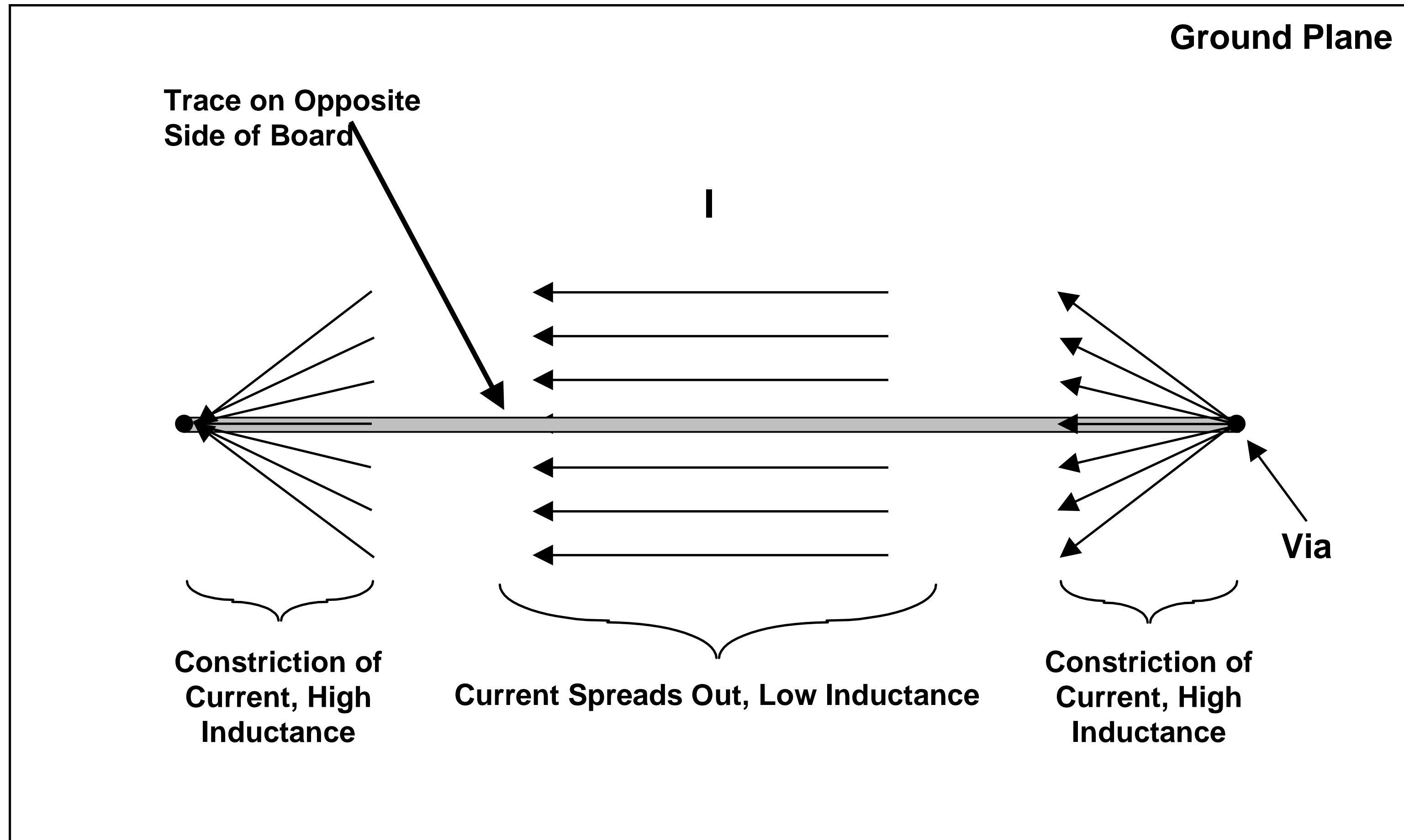
Ground Plane Current Distribution



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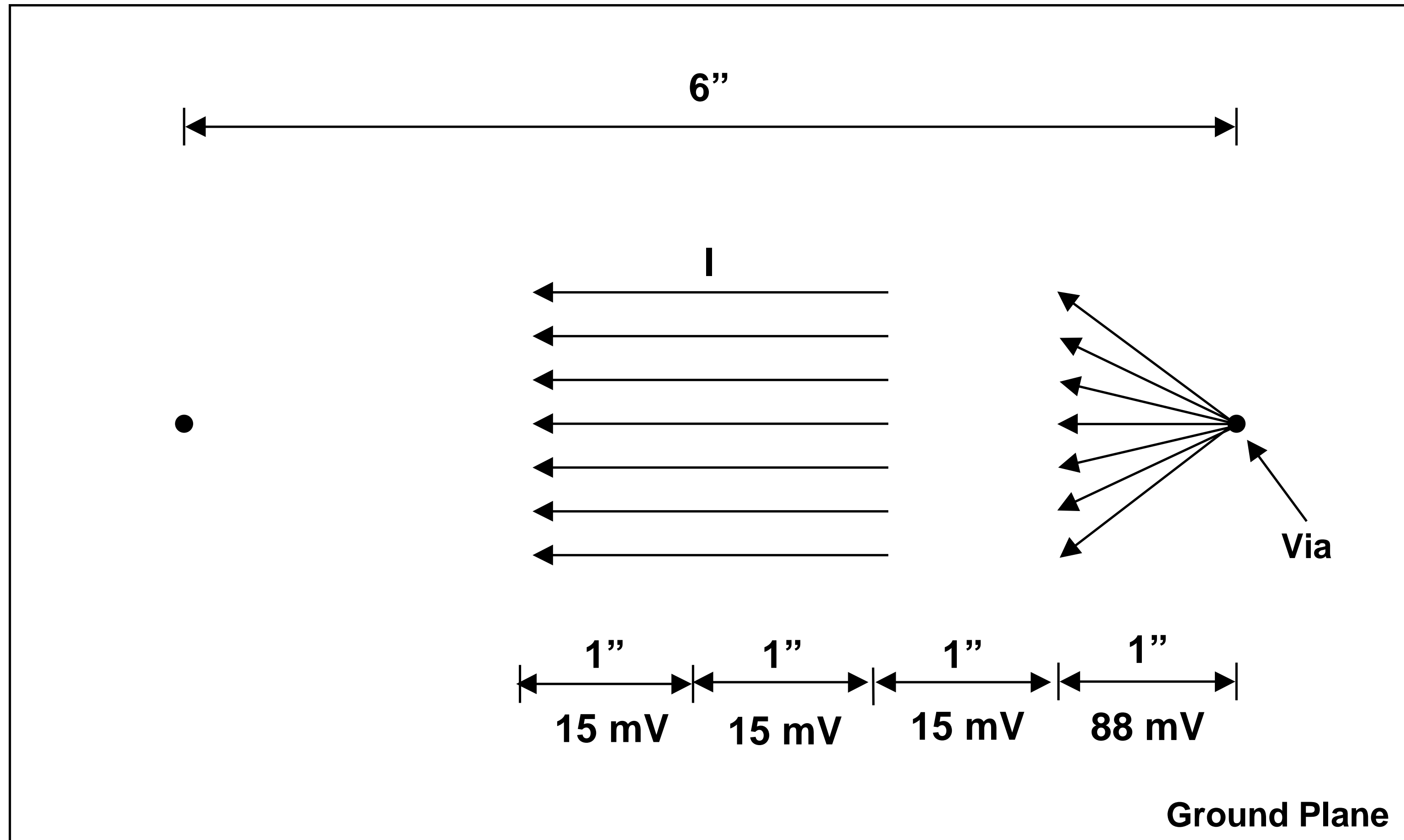
Ground Plane Voltage Measurements
(Peak to Peak Voltage)



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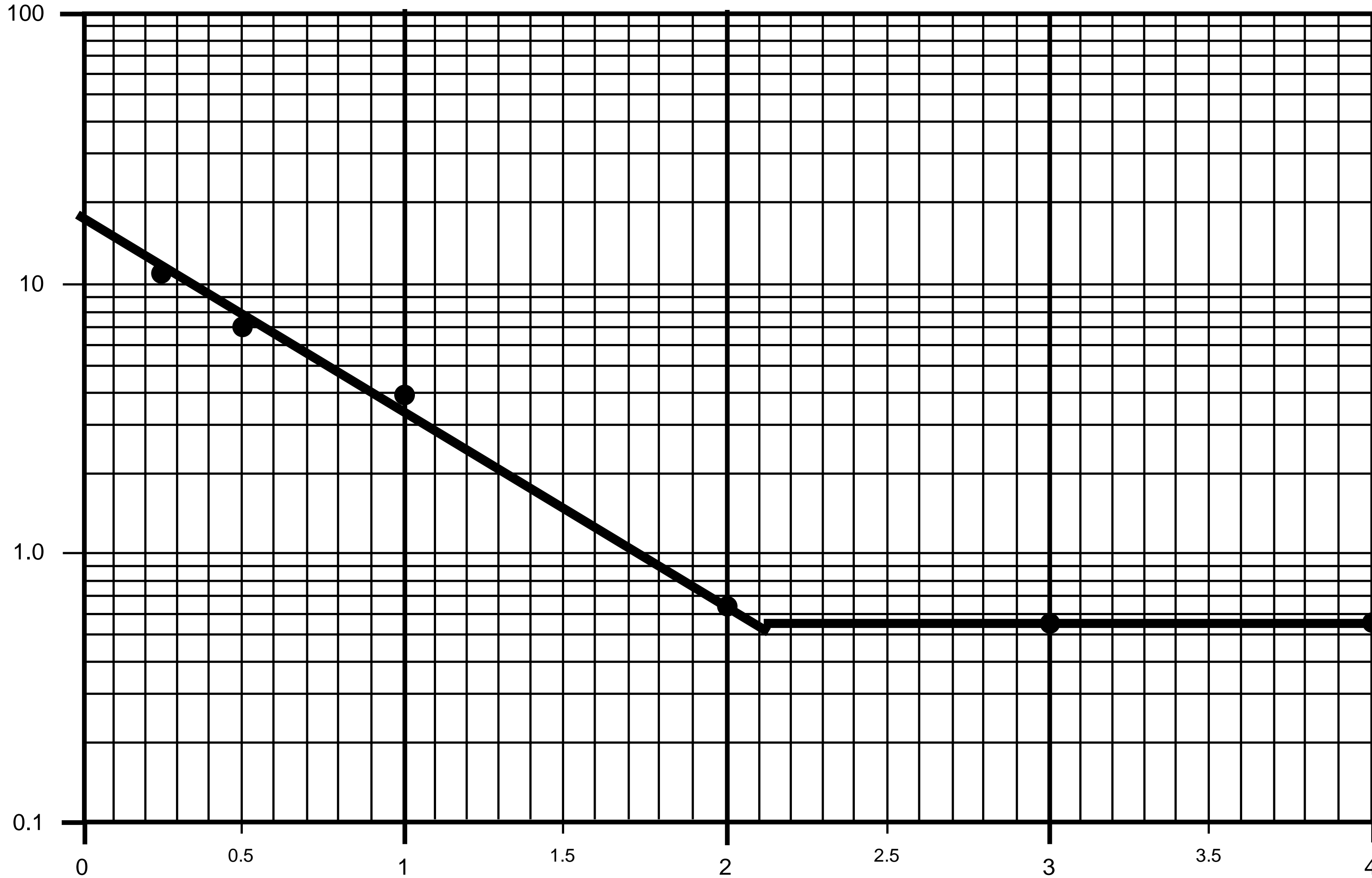
GROUND PLANE INDUCTANCE NEAR VIA



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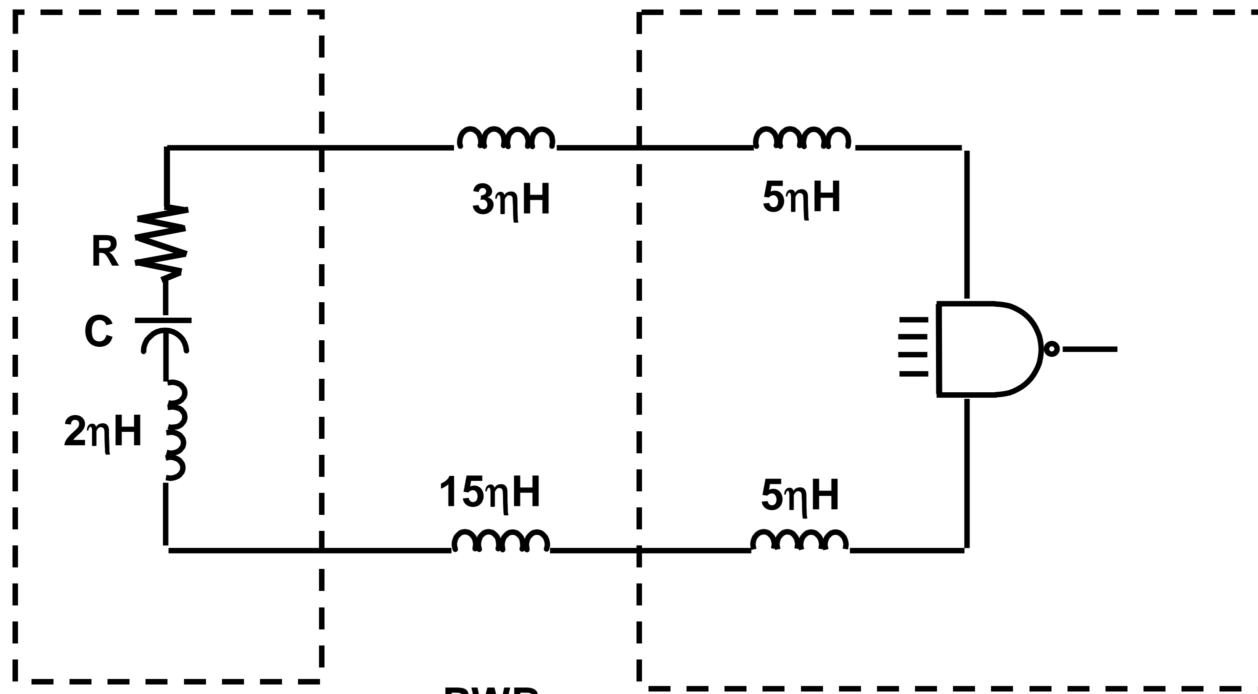
HOC
ELECTROMAGNETIC
COMPATIBILITY

DECOUPLING NETWORK - EQUIVALENT CIRCUIT



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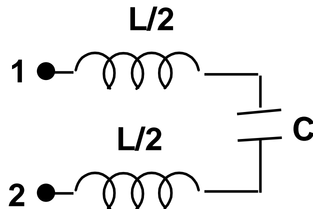
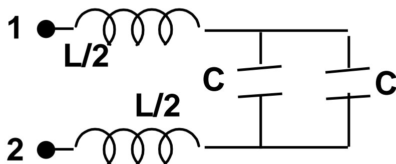
MULTIPLE CAPACITORS



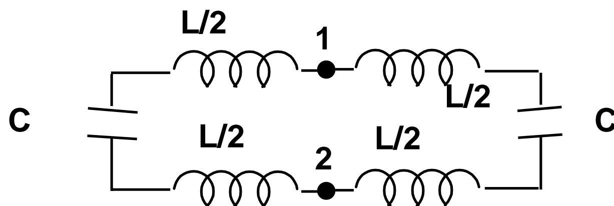
$C_t = C$

$L_t = L$



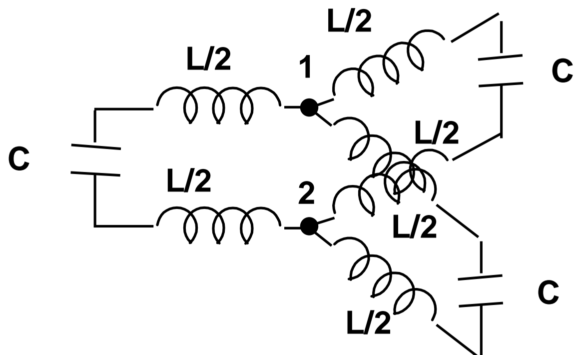
$C_t = 2C$

$L_t = L$



$C_t = 2C$

$L_t = L/2$



$C_t = 3C$

$L_t = L/3$

General Equation

$C_t = NC$

$L_t = L/N$

For N Capacitors of Value C, Each in Series With an Inductance L

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DECOUPLING

- It is Difficult to Achieve Good Decoupling at High Frequencies (> 50 MHz)
- One Way to Achieve This is With Multiple Capacitors (2-50)
  - — Make Them The Same Value
  - — Spread Them Out Physically
- Another Approach is by Using Embedded PCB Capacitance
- Interdigitated Power & Ground Pins Helps Lower the IC Lead Inductance
- One of the Biggest Limitations in Using Decoupling Capacitors is the Inductance of the Pad to Via Trace.
  - — Use Multiple Vias, or
  - — Pad in Via Technology to Reduce This
- Another Approach is to use Multiple Capacitors Inside the IC Package Itself
- Isolated Power Planes Can be Helpful in Minimizing the Bad Side Effect of Poor Decoupling But Does Not Solve the Basic Problem

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SIGNAL INTEGRITY (SI) & EMC

- Signal Integrity: How a Signal Effects Itself
- Signal Integrity: Usually Concerned With Millivolts & Milliamps

- EMC: How a Signal Effects Others
- EMC: Usually Concerned With Microvolts & Microamps

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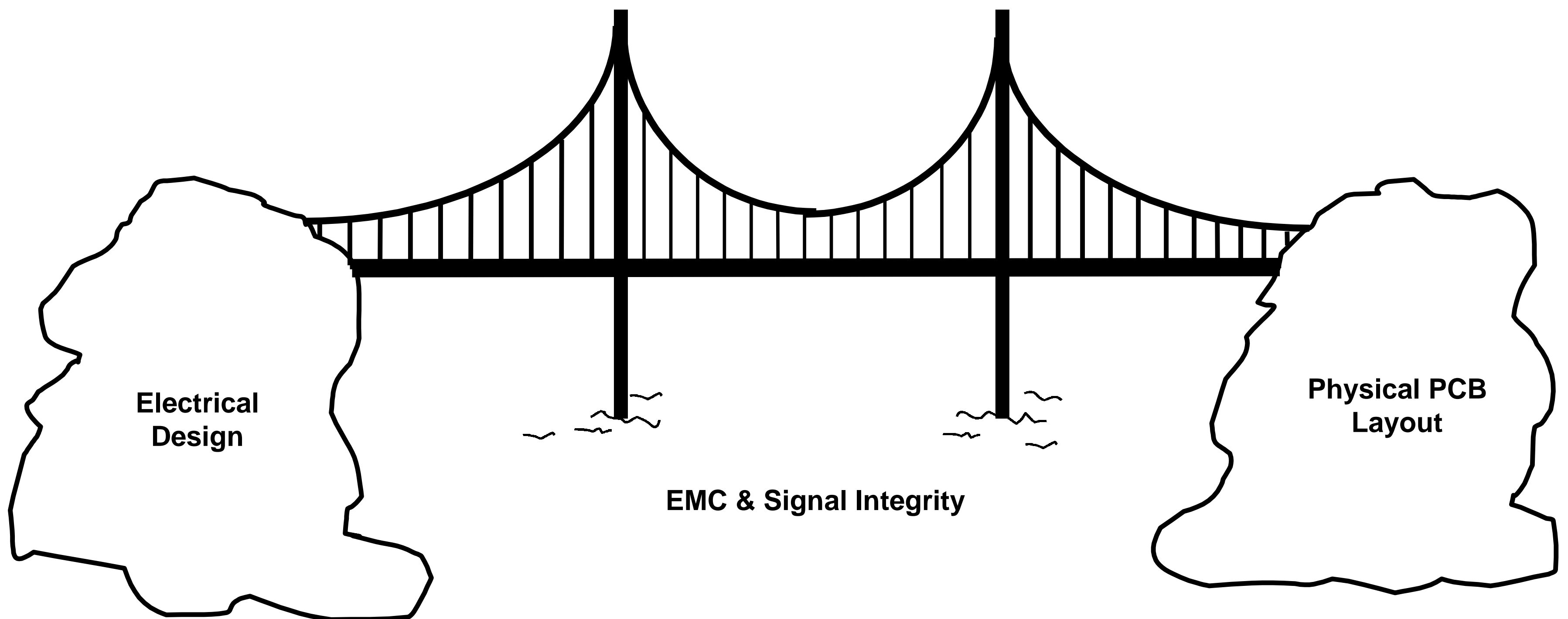
EMC & SIGNAL INTEGRITY



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ELECTRICAL & PHYSICAL PARAMETERS

- Physical PCB Layout
  - Copper
  - Dielectric
  - Traces
  - Vias
  - Pads
- This is What We Build

- Electrical Parameters
  - Inductance
  - Capacitance
  - Resistance
  - Characteristic Impedance
- This is What The Signal Sees

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THERE ARE FOUR SOURCES OF SIGNAL DISTORTION

- The Signal Net Itself
  - Discontinuities
  - Reflections
  - Attenuation
- Crosstalk
- Power & Ground Noise
  - Ground Bounce
  - Decoupling
- External Noise Sources
  - Radiated
  - Conducted

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HIGH DENSITY INTERCONNECT

- Chip Scale Packaging (CSP)
  - Ball Grid Arrays
  - Chip on Board
  - Flip Chip
  - Reduced Pkg. Inductance
- System on a Chip (SOC)
  - Large I/O Counts (>500)
- PCB Layout/Stackup
  - Closer Spaced Layers
  - Elimination of Surface Layer Traces
  - Transmission Lines
  - Faraday Shields
- Testability Issues
  - Test Point Access
- PCB Materials
  - FR-4
  - Polyamide
  - Ceramic/Glass
  - PolyTetraFluroEthelyne (PTFE)
- Vias
  - Microvias (<6 mil)
  - Via in Pad
  - Blind Vias
  - Buried Vias
- Drilling Techniques
  - Laser
  - Plasma
  - Photo-Defined

Denser, Faster, Smaller

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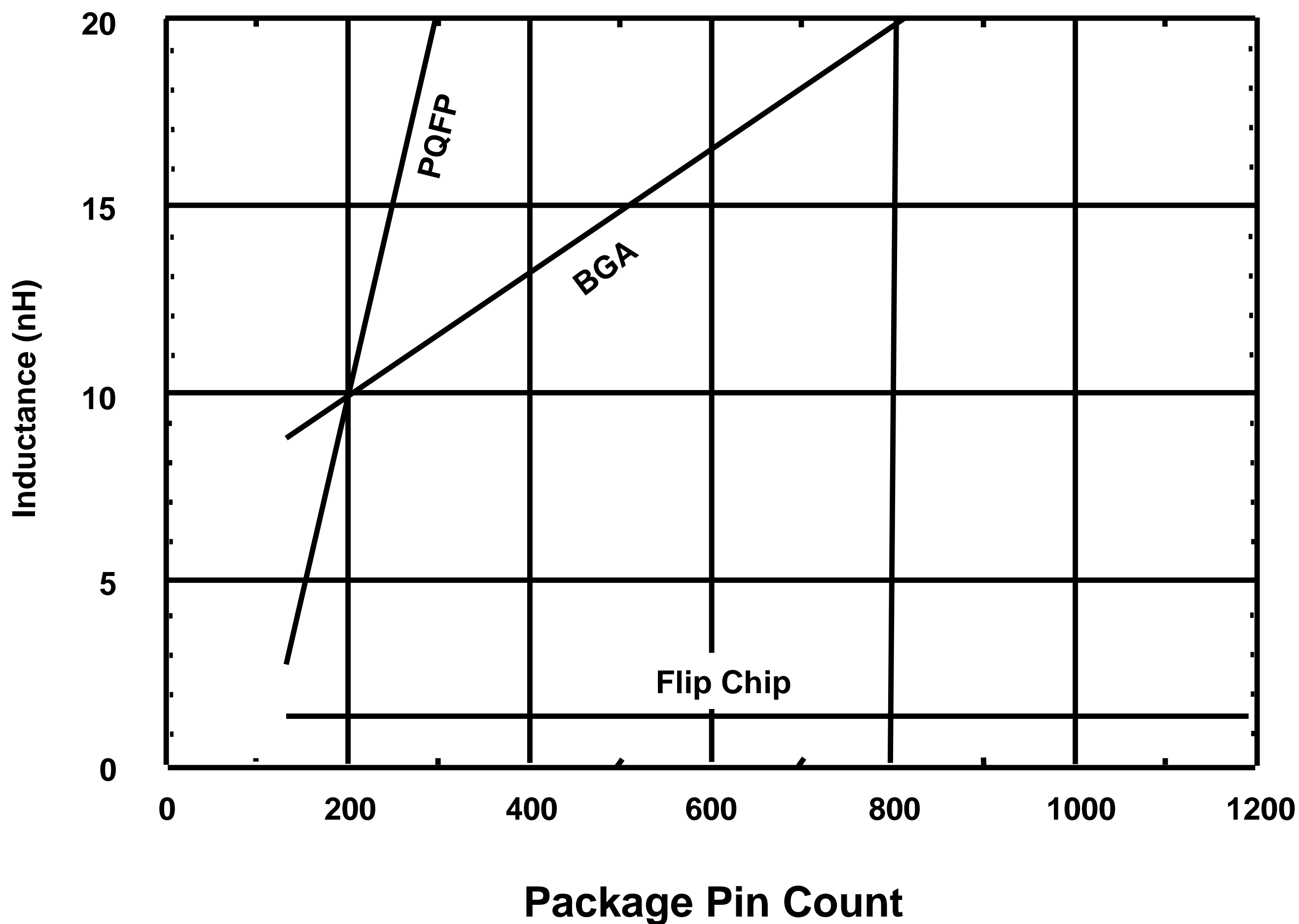
IC PACKAGE INDUCTANCE



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TRANSMISSION LINE LOSSES

- Skin Effect
- Dielectric Loss
- Ground Plane Loss
- Surface Roughness
- Radiation Losses

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SUMMARY
(TRANSMISSION LINE LOSSES)

- For Traces Shorter Than 12” You Can Usually Ignore all Losses up to 1 GHz.
- Above 1 GHz Skin Effect Losses Become Significant
- Above 3 GHz Dielectric Losses Become Predominant

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IN SUMMARY

- The Difference Between Signal Integrity (SI) & EMC is Why You Do Something, Not What You Do
  - For EMC You Do Something to Minimize the Emissions and Susceptibility or For Regulatory Compliance
  - For Signal Integrity You Do The Same Thing to Make the Circuit Work Reliably

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NEW TECHNOLOGY

- Evolution of New Technology
  - — State of the Art
  - — Leading Edge
  - — Commodity
- Embedded Capacitance
- Micro-Vias, Buried Vias. Blind Vias
- Chip Scale Packaging
- New PCB Materials

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BE INNOVATIVE

- Understand the Basic Principles of EMC & SI and Apply them in New Innovative Ways
- Don’t be Afraid to Do Things Differently
- Fund Some R & D With Respect to EMC & SI
- Consider New Technologies
- What’s New Today Will Probably be Common Tomorrow
- Continue to Learn and Educate Yourself
- Remember, Whatever You Did Last Time Will Probably Not Work Next Time

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